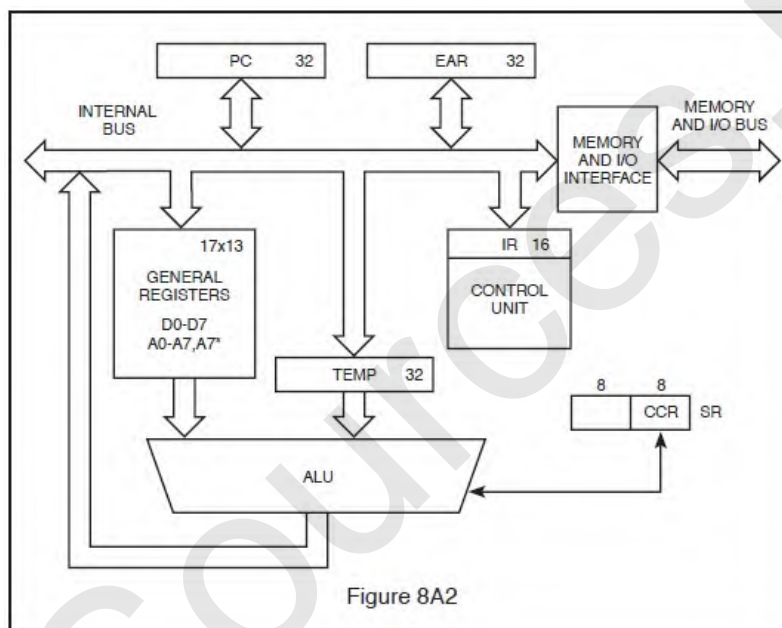
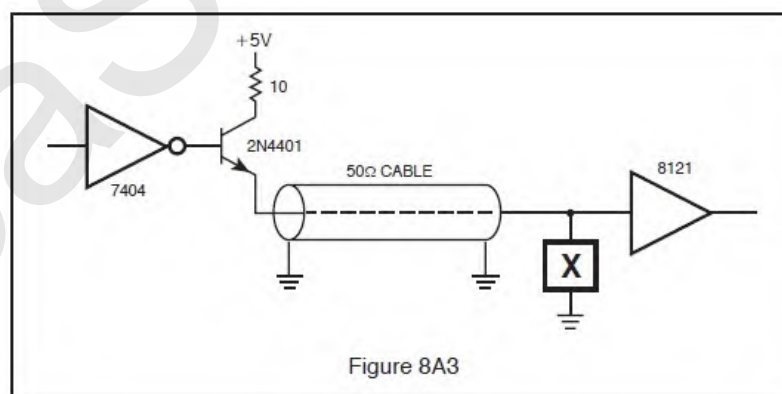


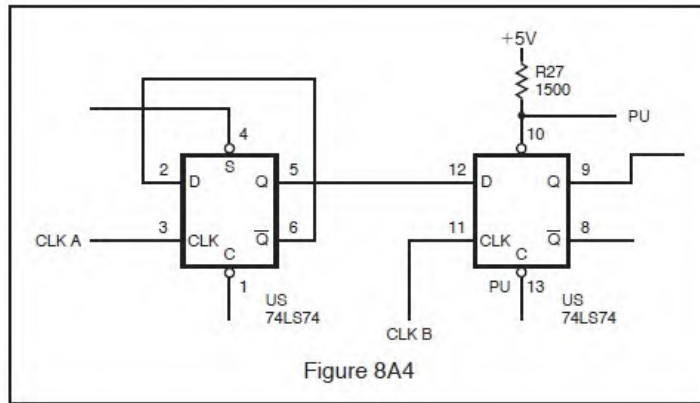
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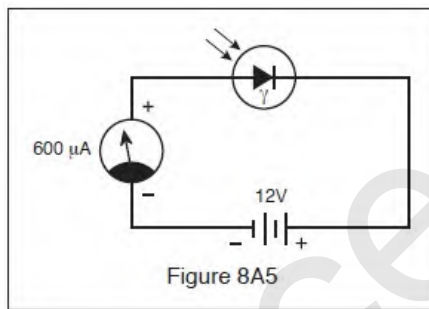
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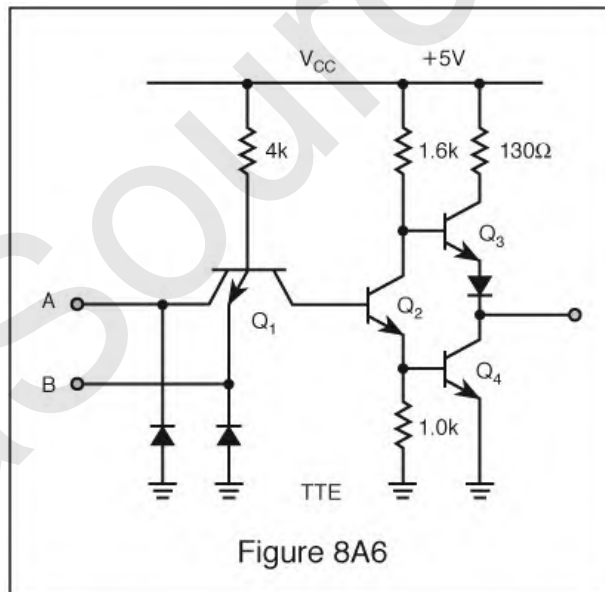
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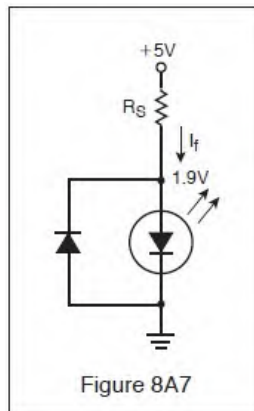
8a4



8a5



8a6



8a7

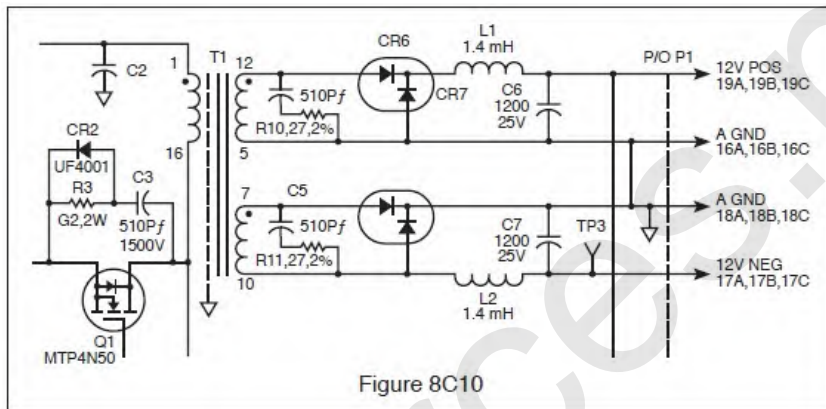
TRUTH TABLE

INPUTS			OUTPUT
\overline{OE}	CP	Dn	\overline{Qn}
L		H	L
L		L	H
L	L	X	No Change
H	X	X	Z

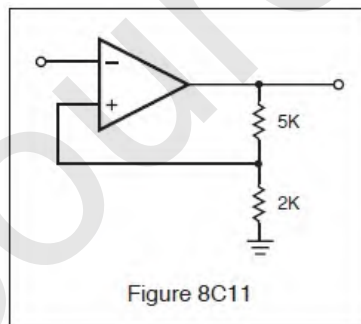
Note: X = Don't care
 Z = High impedance state
 = Low-to-High transition

Figure 8A8

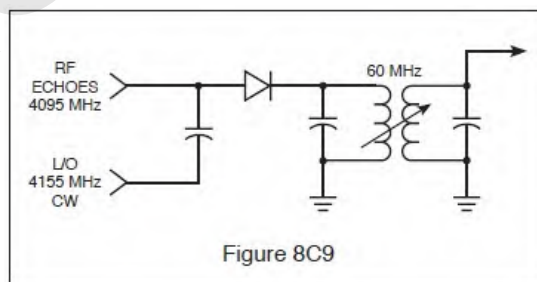
8a8



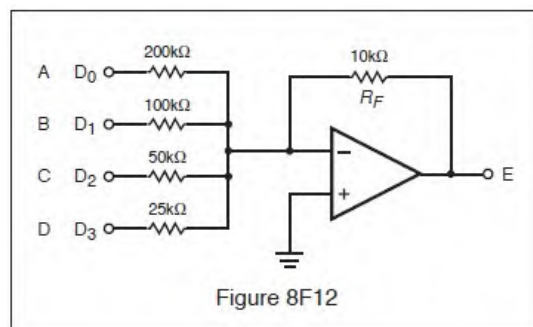
8c10



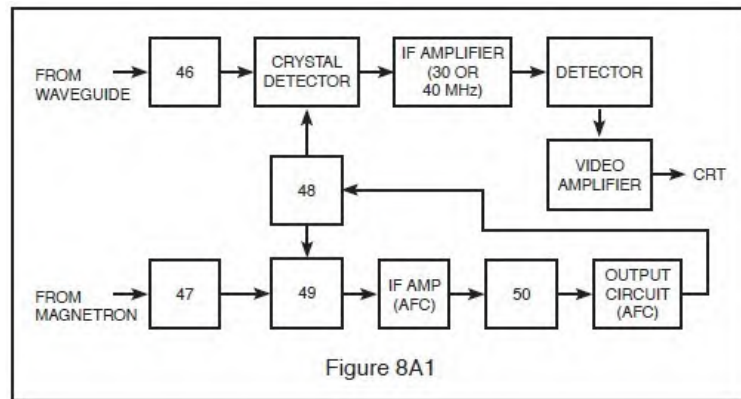
8c11



8c9



8f12



e18a

TRUTH TABLE

INPUTS			OUTPUT
OE	CP	Dn	Qn
L		H	L
L		L	H
L	L	X	No Change
H	X	X	Z

Note: X = Don't care
Z = High impedance state
 = Low-to-High transition

Figure 8A8

e18b

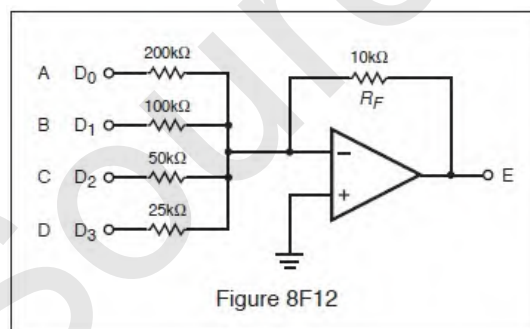
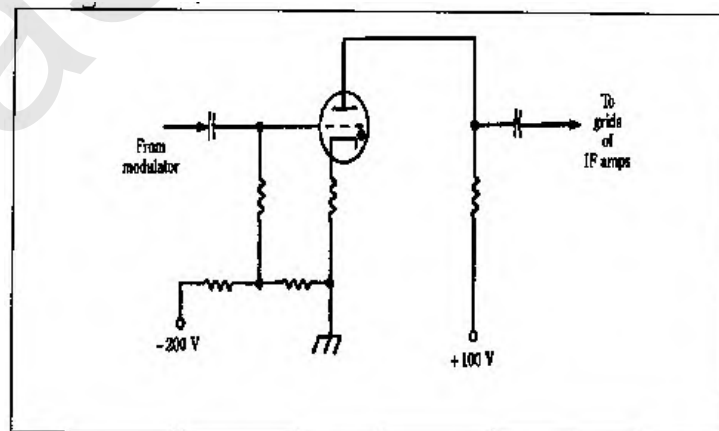
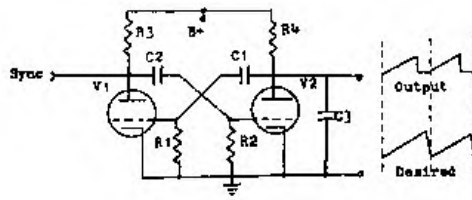


Figure 8F12

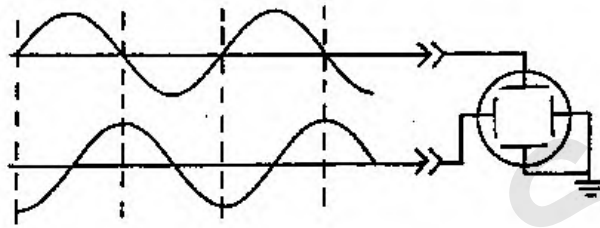
e18c



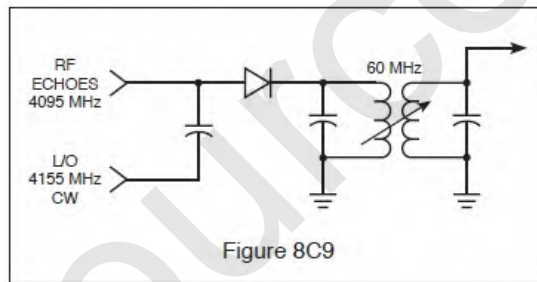
e18d



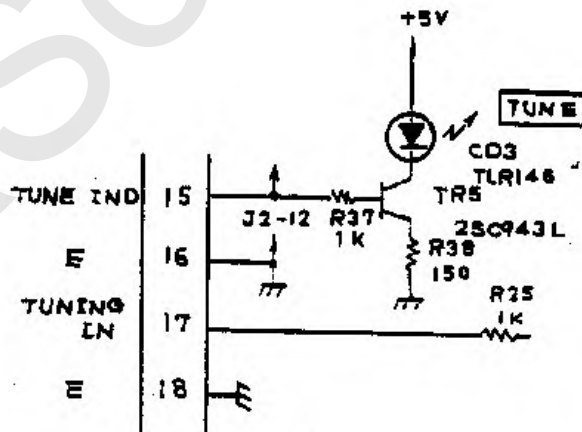
el8e



el8f



el8g



el8h

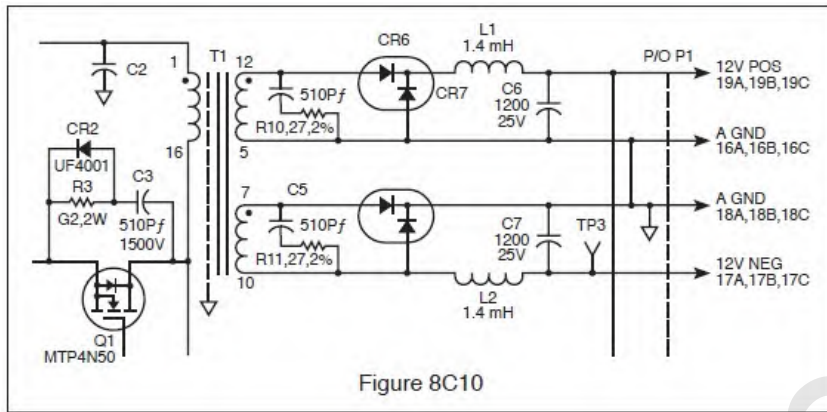


Figure 8C10

e18i

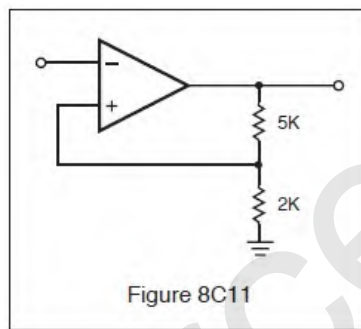
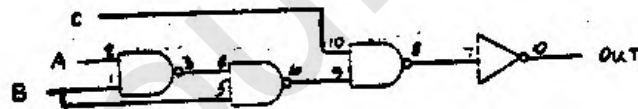


Figure 8C11

e18j



e18k

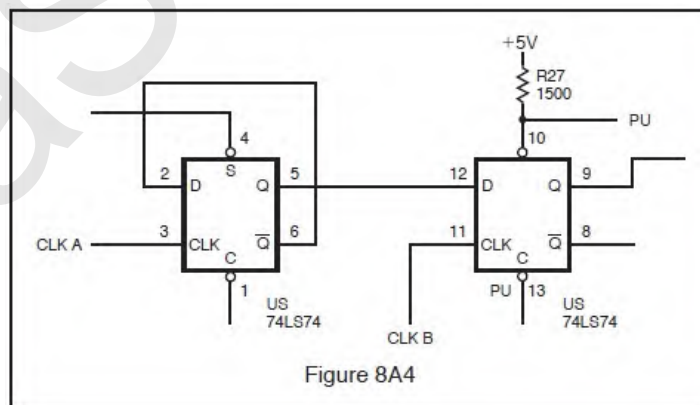
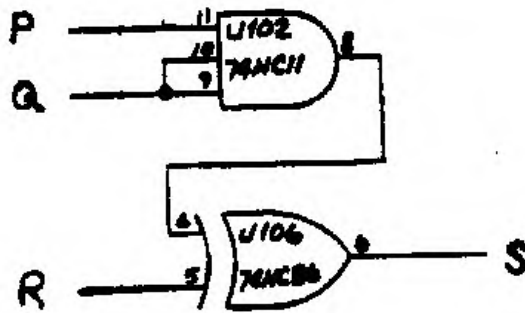
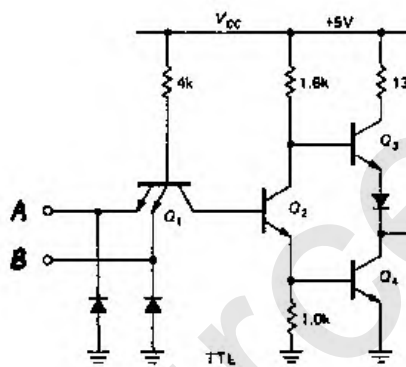


Figure 8A4

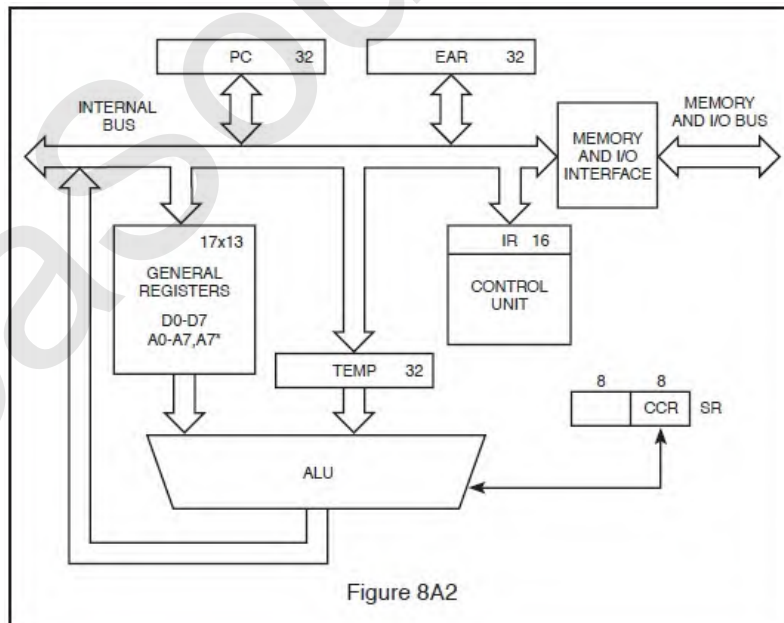
e18l



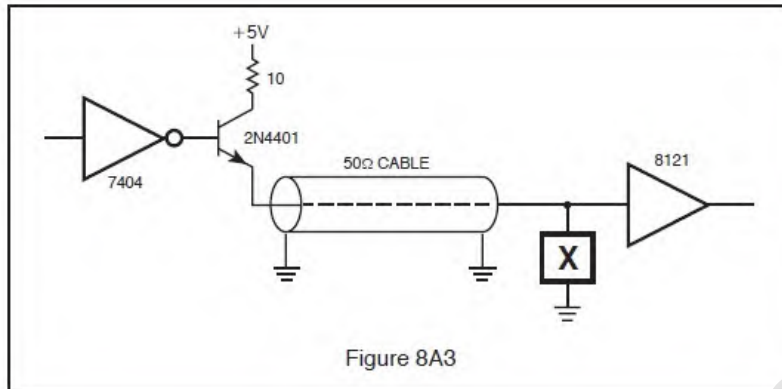
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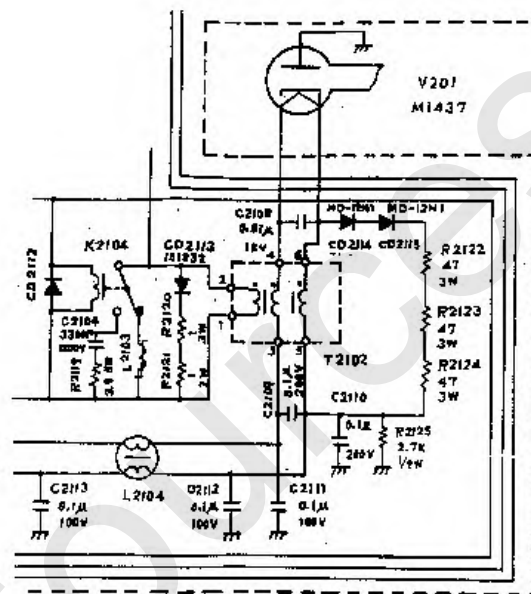
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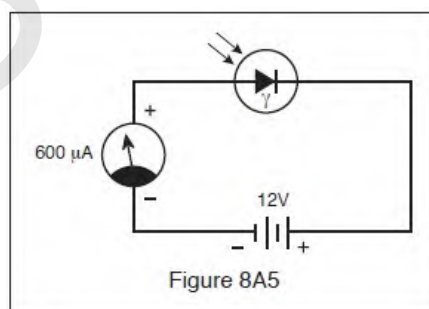
e18o



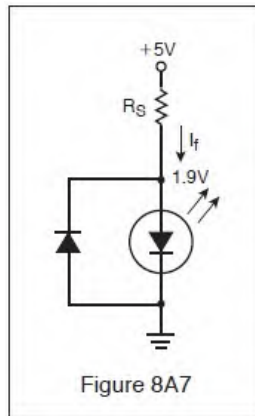
e18p



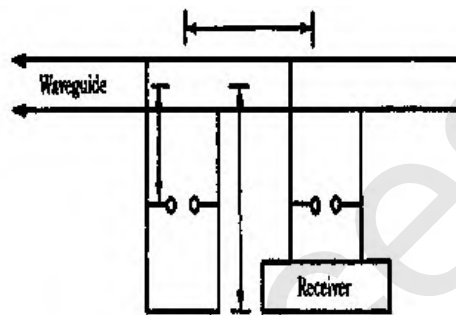
e18q



e18r



e18s



e18t